ST. ALOYSIUS COLLEGE (AUTONOMOUS), JABALPUR

Reaccredited 'A+ 'Grade by NAAC(CGPA:3.68/4.00)
College with Potential for Excellence by UGC
DST-FIST Supported & STAR College Scheme by DBT

Faculty of Science

Bachelor of Science (B.Sc.), I Semester
Subject: Computer Science
Paper-Major/Minor
COMPUTER SYSTEM ARCHITECTURE

Course Outcomes

CO. No.	Course Outcomes	Cognitive Level
CO 1	Understand the basic structure, operation and characteristics of digital computers.	U, A
CO 2	Be able to design simple combinational digital circuits based on given parameters.	K
CO 3	Understand the working of arithmetic & logic unit	U
CO 4	Know about hierarchical memory systems including cache memories and virtual memory.	U, An
CO 5	Understand the concept and advantages of parallelism, multi-processors and multi-core processors.	U

Credit and Marking Scheme

	Credits	Marks		Total Marks
		Internal	External	
Theory	4	40	60	**100**
Practical	2	40	60	**100**
Total	**6**	**200**		

Evaluation Scheme

	Marks	
	Internal	**External**
Theory	3 Internal Exams of 20 Marks (During the Semester) (Best 2 will be taken)	1 External Exams (At the End of the Semester)
Practical	3 Internal Exams (During the Semester) (Best 2 will be taken)	1 External Exams (At the End of the Semester)

ST. ALOYSIUS COLLEGE (AUTONOMOUS), JABALPUR

Reaccredited 'A+ 'Grade by NAAC(CGPA:3.68/4.00)
College with Potential for Excellence by UGC
DST-FIST Supported & STAR College Scheme by DBT

Bachelor of Science (B.Sc.)
I Semester

Subject: Computer Science
Paper: Major/Minor, Computer System Architecture

Content of the Course

No. of Lectures (in hours per week): 2 Hrs. per week

Total No. of Lectures: 60 Hrs. **Maximum Marks:** 60

Units	Topics	No. of Lectures
I	Definition, Characteristics, Block Diagram of a Computer, Input devices - Output Devices Fundamentals of Digital Electronics: Number System-Binary, Decimal, Octal, Hexa-Decimal, Conversions, Binary Arithmetic-Addition, Subtraction, Multiplication, Division, Sign Magnitude, Complements-1's and 2's, Fixed-Point Representation, Floating-Point Representation.	10
II	Computer Memory, Volatile and Non-Volatile Memory, Primary: RAM, ROM, Secondary Memory: Magnetic Disk, Magnetic Tape, Optical Disk, Working of Magnetic Disk and Optical Disk, Introduction to system software: operating system and its functions, Types of operating system.	10
III	Boolean Algebra, Reducing Boolean Expression, Logic Gates-AND, OR, NOT, Universal Gates-NAND, NOR, Analog and Digital Signals, Clock Waveform Timing, Map Simplification, K-Map- Two, Three and Four variables.	10
IV	Combinational Circuits- Adder, Subtractor, Multiplexer, De-multiplexer, Decoders, Encoders. Binary Codes – Gray Codes, ASCII code, BCD code, EBCDIC, Error Detection Code and Correction Code, Hamming Code.	10
V	Sequential Circuits - Flip - Flops, SR, D, T, JK, Master-Slave, Registers, Counters, Instruction, Instruction Format, Instruction Codes, Handshaking, DMA Data Transfer, Auxiliary Memory, Cache Memory, Associative Memory, Flynn's classification - Introduction to SISD, SIMD, MISD, MIMD, Parallelism, Multicore processors.	10

References

Text Books:

- "Computer Fundamentals" by P.K.Sinha, Pearson
- "Computer system Architecture" by M. Morris Mano, Pearson

Reference Books:

- "Computer system Architecture and Organization" by Patterson, McGraw Hill
- "Computer system Architecture & Organization" S.P.S. Saini, S. K. Katheria, Published by Katharia and Sons

Web Links:

- https://www.javatpoint.com/computer-organization-and-architecture-tutorial

ST. ALOYSIUS COLLEGE (AUTONOMOUS), JABALPUR

Reaccredited 'A+ 'Grade by NAAC(CGPA:3.68/4.00)
College with Potential for Excellence by UGC
DST-FIST Supported & STAR College Scheme by DBT

List of Practical

(Digital Electronics)

1. To study basic gates (AND, OR, NOT) and verify their truth tables.
2. To study and verify NAND as a Universal gate using IC 7400.
3. To realize basic gate AND from Universal gate NAND.
4. To realize basic gate OR from Universal gate NAND.
5. To realize basic gate NOT from Universal gate NAND.
6. To study and verify NOR as a Universal gate
7. To realize basic gate AND from Universal gate NOR.
8. To realize basic gate OR from Universal gate NOR.
9. To realize basic gate NOT from Universal gate NOR.
10. Verification and Interpretation of truth table for XOR gate.
11. To study Half Adder using basic gates and verify its truth table.
12. To study Full Adder using basic gates and verify its truth table.
13. To design and construct RS flip Flop using gates and verifies the truth table.
14. To design and construct JK Flip Flop using gates and verifies the truth table.
15. To verify De-Morgan's First Law Theorem.
16. To verify De-Morgan's Second Law Theorem.